CLAIMS

1. A method comprising routing a memory access from a processor core back into the processor core through a bus interface coupled to the processor core.

2. The method of claim 1, wherein said routing comprises:

determining a status of a re-routing bridge in the bus interface;

determining an address of the memory to be accessed; and

placing the access on a bus back into the processor core in response to said bridge being enabled and said address being in a local memory address space.

3. The method of claim 2, wherein said determining the status of the re-routing bridge in the bus interface is enabled comprises checking a status of a bridge-enable bit in a control register.

4. The method of claim 1, further comprising accessing a local memory.

5. The method of claim 4, wherein said accessing local memory comprises writing instructions to a local instruction memory.

6. The method of claim 4, wherein said accessing the local memory comprises accessing a Level 1 (L1) SRAM (Static Random Access Memory).

7. The method of claim 1, wherein said routing a memory access from the processor core comprises routing a memory access from a digital signal processor core.

8. Apparatus comprising:

a processor core including

a local memory including a local data memory and a local instruction memory,

a first port coupled to the local data memory, and

a second port coupled to the local data memory and the local instruction memory; and

a bus interface including

a first bus coupled to the first port,

a second bus coupled to the second port,

a bridge between the first bus and the second bus, and

a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be re-routed into the second port.

9. The apparatus of claim 8, wherein the local memory has an address space, and further comprising a bus control unit operative to switch the multiplexer to the bridge in response to a bridge-enable flag being set and an address of a memory location associated with a memory access from the processor core falls within the local memory address space.

10. The apparatus of claim 8, wherein the local memory comprises a Level 1 SRAM (Static Random Access Memory).

11. The apparatus of claim 8, wherein the first port comprises a fill port and the first port comprises a fill bus.

12. The apparatus of claim 8, wherein the second port comprises a DMA (Direct Memory Access) controller port and the second bus comprises a DMA bus.

13. The apparatus of claim 8, wherein the processor core further comprises an interface coupled to the second port, said interface being operable to access the local data memory and local instruction memory.

14. The apparatus of claim 13, wherein the interface is operable to write instructions to the local instruction memory.

15. An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to route a memory access from a processor core back into the processor core through a bus interface coupled to the processor core.

16. The article of claim 15, wherein the instructions operative to cause the machine to route the memory access include instructions operative to:

determine a status of a re-routing bridge in the bus interface;

determine an address of the memory to be accessed; and

place the access on a bus back into the processor core in response to said bridge being enabled and said address being in a local memory address space.

17. The article of claim 16, wherein the instructions operative to cause the machine to determine the status of the re-routing bridge in the bus interface is enabled include instructions operative to check a status of a bridge-enable bit in a control register.

18. The article of claim 15, further comprising instructions operative to cause the machine to access a local memory.

19. The article of claim 18, wherein the instructions operative to cause the machine to access the local memory include instructions operative to write instructions to a local instruction memory.

20. The article of claim 18, wherein the instructions operative to cause the machine to access the local memory include instructions operative to cause the machine to access a Level 1 (L1) SRAM (Static Random Access Memory).

21. The article of claim 15, wherein the instructions operative to cause the machine to route a memory access from the processor core include instructions operative to cause the machine to route a memory access from a digital signal processor core.

22. A system comprising:

a processor comprising

a processor core including

a local memory including a local data memory and a local instruction memory,

a first port coupled to the local data memory, and

a second port coupled to the local data memory and the local instruction memory; and

a bus interface including

a first bus coupled to the first port,

a second bus coupled to the second port,

a bridge between the first bus and the second bus, and

a multiplexing unit operative to switch between the second bus and the bridge to enable information

placed onto the first bus to be re-routed into the second port; and

a USB (Universal Serial Bus) interface; and

a system bus coupled to the processor and the USB interface.

23. The system of claim 22, wherein the local memory has an address space, and further comprising a bus control unit operative to switch the multiplexer to the bridge in response to a bridge-enable flag being set and an address of a memory location associated with a memory access from the processor core falls within the local memory address space.

24. The system of claim 22, wherein the local memory comprises a Level 1 SRAM (Static Random Access Memory).

25. The system of claim 22, wherein the first port comprises a fill port and the first port comprises a fill bus.

26. The system of claim 22, wherein the second port comprises a DMA (Direct Memory Access) controller port and the second bus comprises a DMA bus.

27. The system of claim 22, wherein the processor core further comprises an interface coupled to the second port, said interface being operable to access the local data memory and local instruction memory.

28. The system of claim 27, wherein the interface is operable to write instructions to the local instruction memory.